REMARKS/ARGUMENTS

Claim1 was rejected as being unpatentable over Thurber, Jr. (U.S. Patent No. 6,169,444). Applicant respectfully traverses this rejection.

The charge pump circuit of the present invention includes a delay circuit (Bl; Fig.3) to increase the voltage conversion efficiency. After a gate voltage (ϕTl) of a first transistor (TR1) is determined to a low level to turn off the first transistor, the delay circuit (Bl) delays the determined voltage (ϕTl) and generates a delayed signal (ϕC1), thereby decreasing a voltage of the node (Nl) between the first and second transistors (TR1, TR2) to the low level. That is, the voltage at the node (Nl) changes after the gate voltage is determined to the low level that turns off the transistor (TR1). Thus, the node Nl voltage does not change while the gate voltage is decreasing, which prevents a large through current from flowing through the transistors (TR1, TR2).

The Examiner states that switches S2 and S4 of Fig. 4 of Thurber, Jr. correspond to a delay circuit of the present invention. Although there is no detailed description regarding the operation of the switches S1-S4 in the patent publication of Thurber, Jr., it is believed that they do not function as the delay circuit of the present invention. Switches (S1, S2) and switches (S3, S4) appear to operate substantially synchronously without delay to perform a boost operation. Generally, since a clock signal, which is provided to the switches S1 and S2, is provided to the switches S3 and S4 via an inverter, the clock signal is delayed. Thurber, Jr. does not specifically teach the delay of the clock signal caused by using the inverter. Two cases are discussed below: (A) when a delay is considered, and (B) when a delay is not considered as follows:

(A) When a delay is taken into consideration:

Assuming that the switches Sl and S2 are turned on and the switches S3 and S4 are turned off, when the switches S1 and S2 are turned on, there is a state where all the switches S1-S4 are instantaneously turned off because a delayed clock signal is provided to the switches S3 and S4. Then, the switches S3 and S4 are turned on in response to the delayed clock signal, thereby charging a boosted voltage 2V-IN in a capacitor C-X.

In contrast, assuming that the switches S1 and S2 are turned off and the switches S3 and S4 are turned on, when the switches S1 and S2 are turned off, there is a state where all the switches S1-S4 are instantaneously turned on because a delayed clock signal is provided to the switches S3 and S4. At this time, a voltage V-OUT is substantially the same as the voltage V-IN, so that a boosted voltage 2V-IN cannot be generated. Then, the switches S3 and S4 are turned off in response to the delayed clock signal, thereby charging a boosted voltage V-IN in a capacitor C-OUT.

Accordingly, a boosted voltage cannot be properly generated when a delay is taken into consideration, and the Thurber circuit therefore does not disclose the delay circuit as claimed.

(B) When a delay is not taken into consideration:

Since the inverter of Thurber only inverts a clock signal as a control signal, the switching operations of switches S1 and S2, and of switchesS3 and S4 are performed substantially synchronously. Accordingly, the switches S2 and S4 do not function as the delay circuit of the present invention.

As discussed above, since Thurber, Jr. does not teach or suggest the delay circuit of the present invention, the clock signal provided to the switch S1 is not delayed, thus no delayed clock signal is provided to a node between the switches S1 and S2 (terminal of the capacitor C-X).

Claims 2, 3, 6 and 9 were rejected as being unpatentable over Thurber, Jr. In view of Mukainakano et al. (U.S. Patent No. 6,107,862). Applicant also respectfully traverses this rejection.

Since Mukainakano et al. does not teach or suggest the delay circuit of the present invention, this reference fails to cure the deficiencies in Thurber. Thus, the rejection under Section 103 should be withdrawn.

Applicant gratefully acknowledges the allowability of claims 4, 5, 7, 8, 10 and 11.

Based upon the foregoing, Applicants believe that all pending claims are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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